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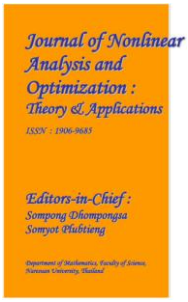

MULTI-BIT DIGITAL COMPARATOR PERFORMANCE ANALYSIS BASED ON CMOS

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ABSTRACT
This paper presents the creation and analysis of various comparators like EXOR/EXNOR. The comparator's structure can be divided into two techniques or modules. The Comparison Evaluation Module (CEM) is the first technique/module, while the Final Module is the second technique/module (FM). The parallel prefix tree structure used by the Comparison Evaluation Module (CEM) is designed to execute a bitwise comparison of two N-bit operands, A and B. Based on the output of the Comparison Evaluation Module, the Ultimate Module (FM) is meant to provide the final outcome (CEM). To obtain the results of multiple comparators utilizing the 45 nm complementary metal oxide semiconductor (CMOS) technology, simulation results are evaluated using the LTspice software. The performance of the multiple comparators like EXOR/EXNOR is analyzed by calculating the total delay, number of transistors in the comparator, power dissipation and current value.

Keywords:
Comparators, AND Gates, NAND Gates, NOR Gates, EXOR Gates, EXNOR Gates.

1. Introduction
The key design component for applications in which the comparison of the outputs of a comparison evaluation module yields the final results is a digital comparator.
Numerous applications exist, including scientific ones like digital image processing, pattern recognition/matching arithmetic sorting, data compression, and applications like digital neural networks and test circuits. The memory addressing logic, queue buffers, and test circuits in computer architecture are all developed using the digital comparator design as a major component. The more the comparator's logic is used in various computation-based designs, the more area, power, and speed may be optimized. Some comparators are designed using dynamic logic to achieve low power consumption; however the restriction of low speed and inadequate noise margin makes the design difficult. The digital comparator logic structure is designed using various logic gates. A logic gate is a device that acts as building block for digital circuits. There are seven basic logic gates such as, AND gate, OR gate, NAND gate, NOR gate, EXOR gate, EXNOR gate and NOT gate. The digital comparator structure uses the NAND, NOR, AND, EXOR and EXNOR logic gates. To perform digital comparator the logic gates EXOR and EXNOR plays an important role. There are many applications of EXOR gate such as it is used in Arithmetic operations, Parity Checker, Controlled Inverter, Binary to grey conversion, Combinational logic circuits minimization and digital comparator. The performance of digital comparators is analyzed by using different EXOR and EXNOR logic gates in digital comparator. Based on the performance the area efficient, power efficient and delay efficient digital comparator is identified. The different EXOR and EXNOR based circuits used in the digital comparator consists of pass transistor logic and CMOS logic to get the better results. The improvement of the scalability and reduction of the delay has been achieved by using the prefix tree structure-based

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comparator that is composed by using 2-bit comparators in each level. For the wide input operands, the comparator
structures are prohibitive due to large delay and power consumption arising from comparison levels. To improve the limiting factors of parallel prefix tree structure such as area and power can be achieved by using two input multiplexers at each level and it generates propagate logic at the first level. Most of the comparators use the pipelining and power down approaches for improvement of speed and power consumption reduction. For improving the operating speed an alternate structure that uses priority encoder-based magnitude decision logic. This structure uses the two pipelined operations which are synchronized with the rising and falling edges of the clock signal to eliminate long dynamic logic chain to improve the delay parameter. In a circuit, logic gates will make decisions based on a combination of digital signals coming from its inputs. Most of the logic gates have the two inputs and one output. Logic gates are based on Boolean algebra. Every terminal is having two binary conditions false or true. False represents 0 and true represents Depending on the type of the logic gates being used and the combination of inputs, the binary output will differ. Logic gates are commonly used in Integrated circuits(IC). The EXOR and EXNOR gates are commonly used in the design of the digital comparators.

2. Comparison process for N-bit Digital Comparator

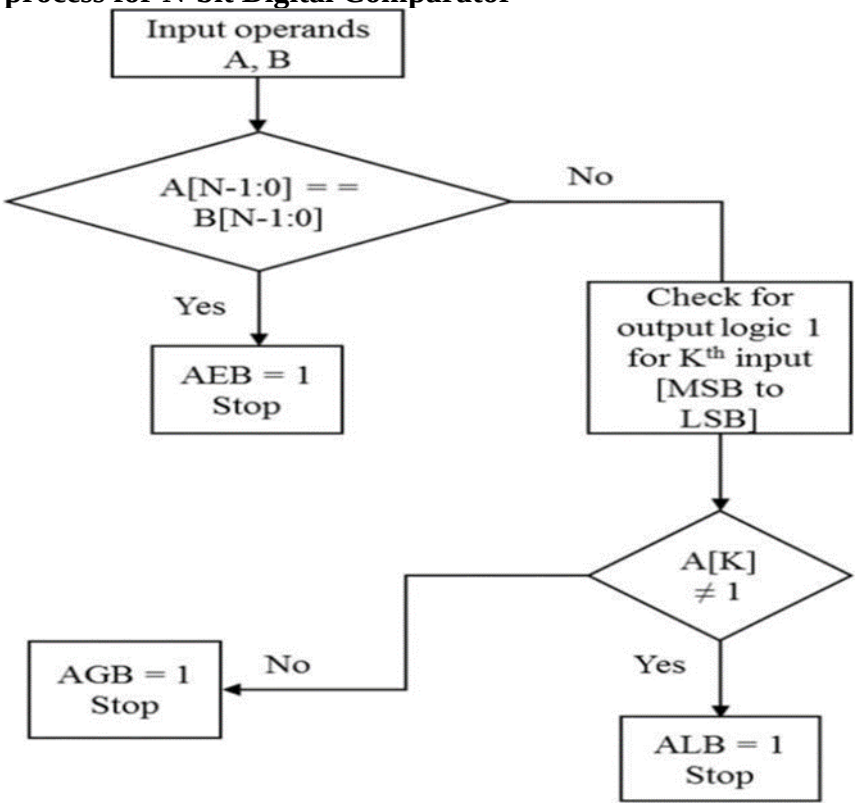

Fig. 1 Flowchart of N-bit digital comparator

The working principle of conventional comparison is shown where the operands A and B have unequal most significant bit (MSB). The two N-bit operands A and B are compared and are checked whether the operands are equal or not equal in bitwise comparison process. The comparison process starts from the $(N-1)^{th}$and it follows the $(N-2)^{th}$ bit and this process will stop when the MSB bits of two operands are equal. If the result is equal then the logical output is AEB condition. If the result of the comparison is not equal of the two MSB bits of the two operands then the pre-encoder output bits are checked from MSB To LSB bits. The output logic ALB or AGB goes to logic 1 based on the results from the pre-encoder. The equal and unequal bit pairs are realised as,

$$X=A\ B, E=A.B$$

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3. Design Methodology of the digital comparator EXOR/EXNOR Gate using 24 transistors:

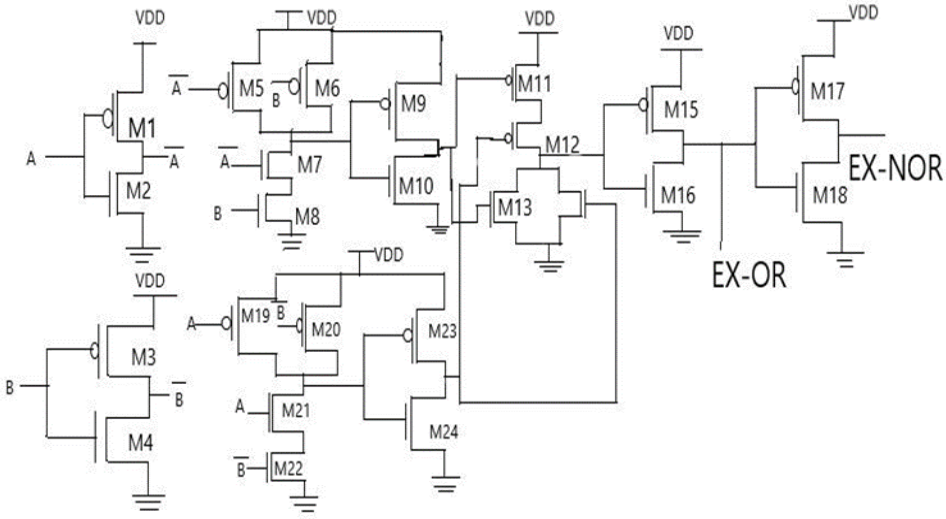

Fig. 2 Schematic diagram of EXOR/EXNOR gate circuit

The EXOR/EXNOR circuit have the 24 transistors. This 24 transistors circuit uses the CMOS logic. The circuit is having the 12 PMOS and 12 NMOS transistors. When logic 0 is applied as the input to both the transistors the PMOS transistor will ON and the NMOS transistor will OFF.And the other case is that when the input applied is logic 1 then the PMOS transistor will OFF and the NMOS transistor will ON. First the two AND gates are connected and then the output of this is given as the input to the OR gate from this we get the EXOR output, for this CMOS Inverter is given then the EXNOR output will come. The main disadvantage of this circuit is the more number of transistors are used having the more area. Nowthe simplified circuit of EXOR/EXNOR gate with less number of transistors are designed.

EXOR/EXNOR[1] Gate:

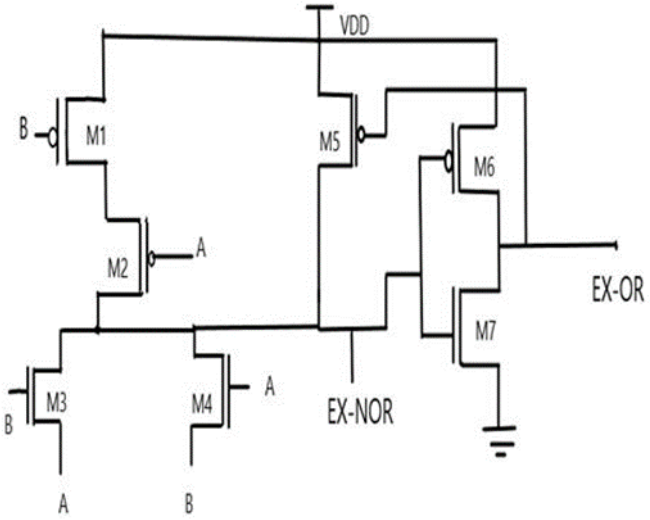

Fig. 3 Schematic diagram of EXOR/EXNOR[1] gate circuit

The EXOR/EXNOR circuit consists of 7 transistors. This circuit uses the CMOS logic. It uses the 7 transistors for EXOR and EXNOR operations as compared with the conventional 24 transistors model. The EXOR and EXNOR circuits has 4 PMOS transistors and 3 NMOS transistors. When the input is applied as logic 0 the PMOS transistors will be in ON condition and NMOS is in OFF condition, when the input is applied as logic 1 the NMOS transistors will be in ON condition and the PMOS is in OFF condition. The M5 transistor is used in the circuit to obtain the full output voltage swing when the applied inputs are (0,0,) or (1,1). The aspect ratio of the consists of 4 PMOS and 3 NMOS transistors which are used to avoid the universal drive constraint faced by the pass transistor logic. The EXOR/EXNOR circuit uses the PMOS transistor in the feedback to maintain the logic level on the

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EXNOR output terminal and the CMOS logic is used to boost up the output to achieve the full voltage swing on the EXOR output terminal. The outputs of the EXOR/EXNOR circuit provides the termination and comparison bits.
The model of the 8 transistors uses the 8 transistors for EXOR and EXNOR with cross-coupled PMOS. This model is used to get the design of the proposed level-1 comparator sub block. This is the best one to get low power and small area.

EXOR/EXNOR[3] Gate:

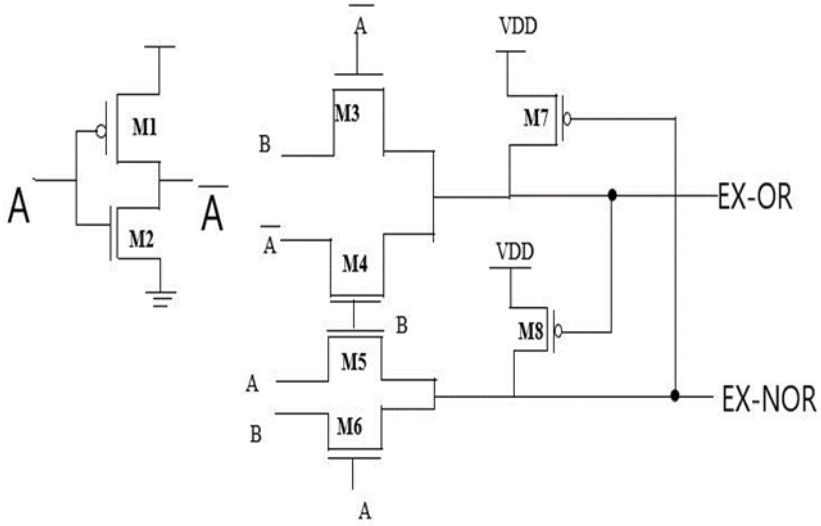

Fig. 4 Schematic diagram of EXOR/EXNOR[3] gate

An eight transistor EXOR/EXNOR with cross coupled PMOS as shown in the figure.This circuit is used to design the three main sub blocks in different stages. The first block is the XE block and the second block is the level-1 comparison block and the third block is the level-2 comparison block.XE block performs the single bit comparison and it gives the outputs through X and E output pins as shown in figure. This is best forlow power and small area as compared to other circuits. 90nm technology is used to design the proposed 64 bits comparator. The Inverters are used in the circuit blocks of XE block, Level-1 comparison block and level-2 comparison block in the designing are of the small size. The eight transistor XE block occupies the small area of 9.75(.
The EXOR/EXNOR circuit consists of 8 transistors. This eight transistors EXOR /EXNOR circuit uses the pass transistor logic and CMOS logic. In the above shown circuit the transistors like M3, M4, M5, M6 uses the pass transistor logic. The EXOR/EXNOR circuit uses the 3 PMOS transistors and 5 NMOS transistors. When the input is applied as logic 0 the PMOS transistor will ON and the NMOS transistor will OFF. If we applied the input as the logic 1 then the PMOS transistor will OFF and the NMOS transistor will ON. Pass transistor logic is compared on the use of MOSFET'S as switches rather than inverters. This logic involves the NMOS and PMOS transistors to transfer the charge from one node to another node under the control of MOS gate voltage. Pass transistors logic uses fewer number of transistors when compared to the fully complementary CMOS logic as the functioning is same in both the designs.

EXOR/EXNOR[4] Gate:

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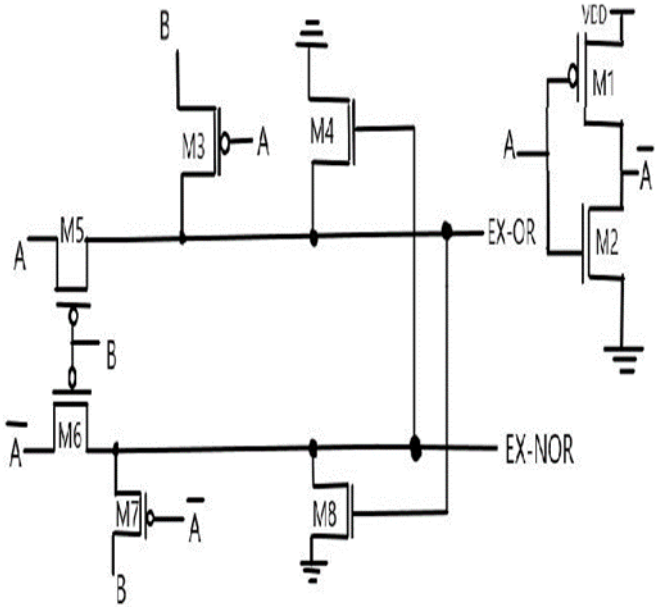

Fig. 5 Schematic diagram of EXOR/EXNOR [4] Gate

The EXOR/EXNOR operation is based on the operation of the pass transistor logic. This circuit consists of eight transistors which gives the output of the EXOR and EXNOR. This method has the advantage of using the less number of transistors by 6 compared with the conventional 14 transistor model. In this model we are using the six transistors that are named as the M1-M6 as shown in the figure. This circuit is using the four PMOS transistors and two NMOS transistors by excluding the two transistors used in the inverter circuit. The limitation of the pass transistor logic is the conventional drive can be optimally minimised by the design of the PMOS and NMOS transistors. It minimizes the power dissipation and the area. This circuit is having the advantage of the limited speed operation. When we apply the input as the logic 0 then the PMOS transistor will ON and the NMOS transistor will OFF, and the other input applied as the logic 1 then the PMOS transistor will OFF and the NMOS transistor will ON. The limitation of the pass transistor logic to overcome the conventional drive by designing the PMOS and NMOS. To boost driving capability this topology uses the cross coupled connection logic. Pass transistors logic uses the fewer number of transistors it done the same function as the fully complementary CMOS logic.

4.Circuit description of the 4-bit digital comparator

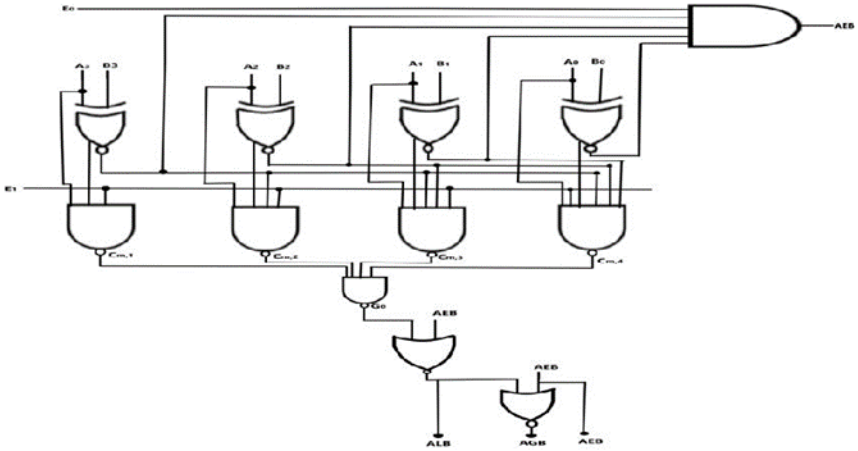

Fig.6 Schematic diagram of 4-bit digital comparator

The operation of the 4-bit comparator is as follows, It has the two modules, they are classified in to two types as, comparison evaluation module (CEM) and final module (FM). It has the five sets the first four sets are in the operation of the comparison evaluation module and the final set is belongs to the final module and this module is the decision module which takes the decision from the comparison

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evaluation module. In the set1 we take the two 4-bit binary operands and compare these two operands bitwise which is carried out by the EXOR/EXNOR cell.
The outputs of the EXOR/EXNOR cells gives the termination and comparison bits which are intended for sets 2 and 3 structures. In the set 2, the AND operation is performed between the equal flag bits and terminated bits from the set 1. In set 3 it contains the cells and combines the set 1 and set 2 outputs and performs the NAND operation. In set 4 it contains the NAND type logic cells and the inputs received from the set 3 and set 4 have requires (N/4) cells to combine the outputs of the set 3 in the each partition of the set. In the set 5 it contains two NOR-type logic cells to decide the final results of the digital comparator. The first NOR gate uses the outputs of set 4 and AEB as the inputs to decide the ALB, where second NOR gate uses the output of first NOR gate and AEB as inputs to decide the AGB. 4-bit digital comparator uses the many of the EXOR/EXNOR gate.

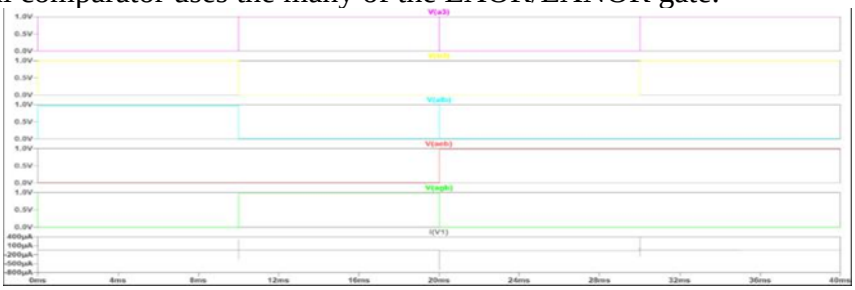

Fig. 7 waveform of 4-bit comparator using EXOR/EXNOR

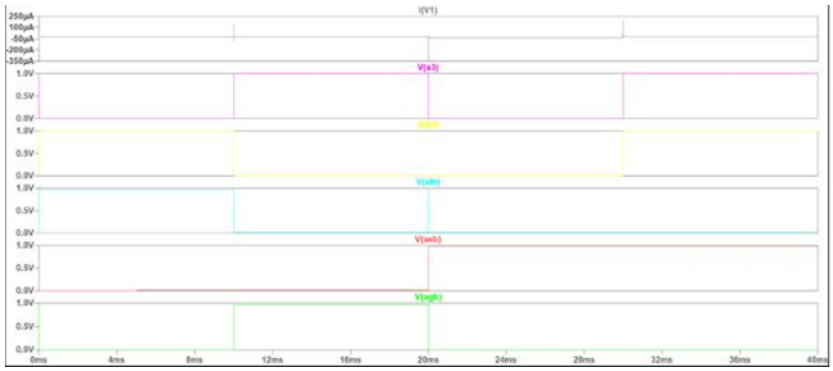

Fig. 8 waveform of 4-bit comparator using EXOR/EXNOR [1] gate

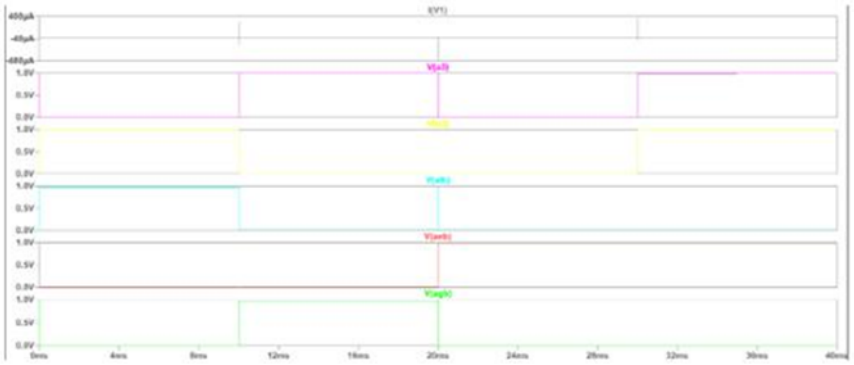

Fig. 9 waveform of 4-bit comparator EXOR/EXNOR [3] gate

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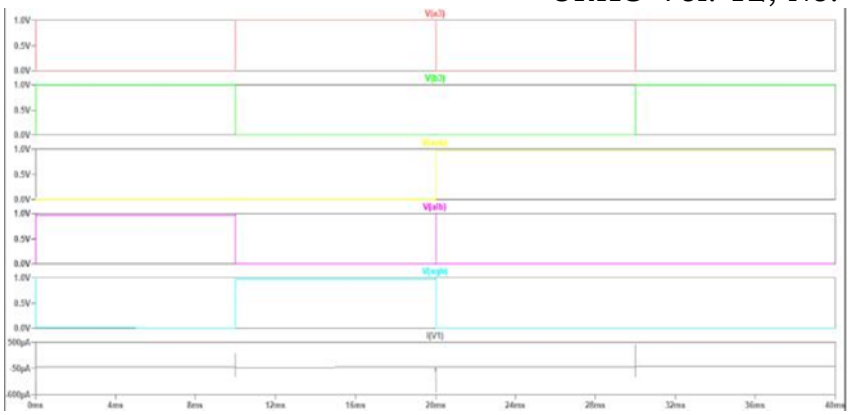


Fig. 10 waveform of 4-bit comparator EXOR/EXNOR [4] gat

8-bit digital comparator:

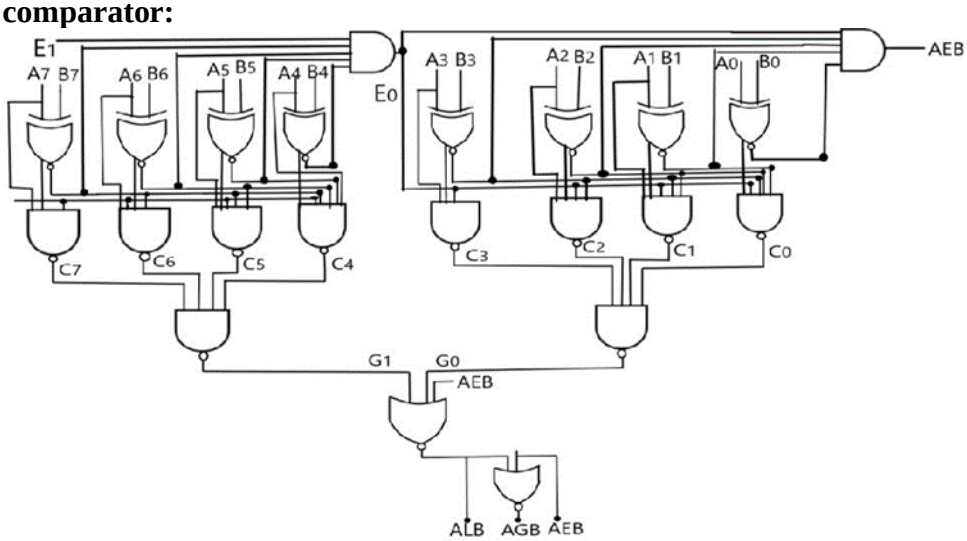


Fig. 11 Schematic diagram of 8-bit digital comparator

This circuit is the cascading form of the 4-bit digital comparator. It has the same operation as the 4-bit digital comparator but the outputs from theeach block of the NAND gates are given to the NOR gates and the inputs of this NOR gate is the AEB and the outputs from the two blocks of the NAND gate. This gate decides the output is AEB or ALB or AGB.

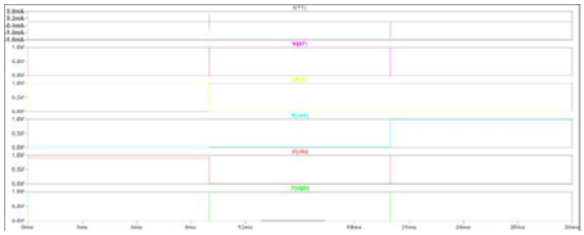
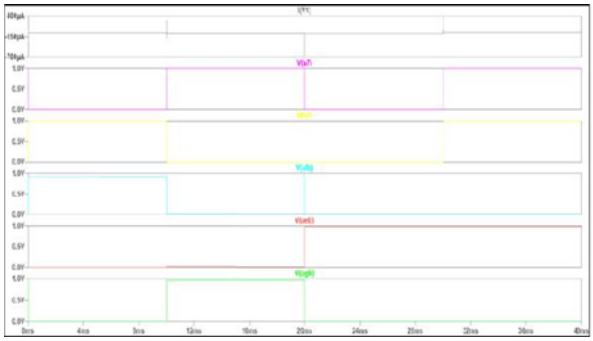


Fig. 12 waveform of 8-bit comparator EXOR/EXNOR gate



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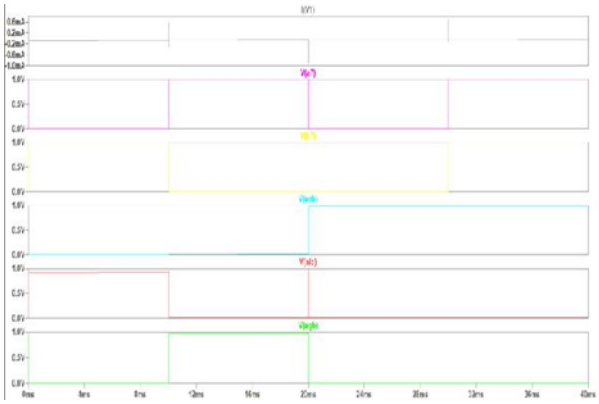

Fig.14 waveform of 8-bit comparator EXOR/EXNOR[3] gate

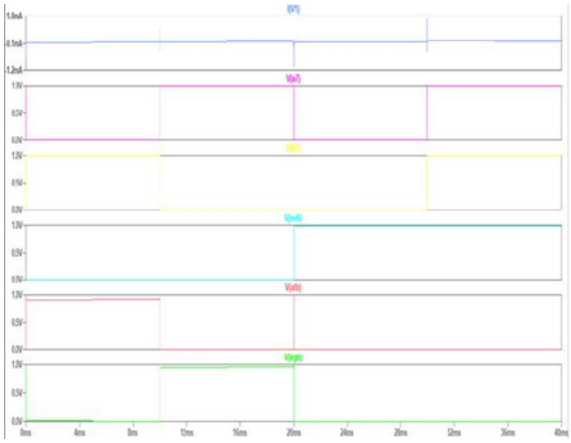

Fig. 15 waveform of 8-bit comparator EXOR/EXNOR[4] gate

16-bit digital comparator:

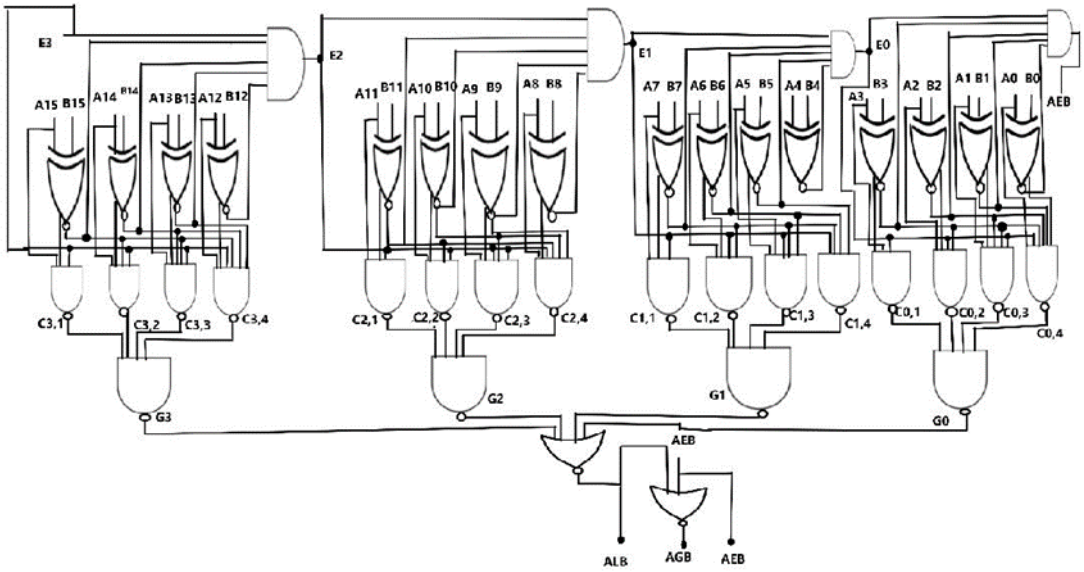

Fig.16 Schematic diagram of 16-bit digital comparator

This is the cascading form of the 8-bit digital comparator. In this the outputs from the each blocks of the NAND gates are given as the input to the NOR gate. This NOR gate has the inputs of AEB and the outputs of NAND gates. And this output of the NOR gate is given as the input to the another NOR gate which compares the three conditions and gives the outputs as the AEB, ALB,AGB.

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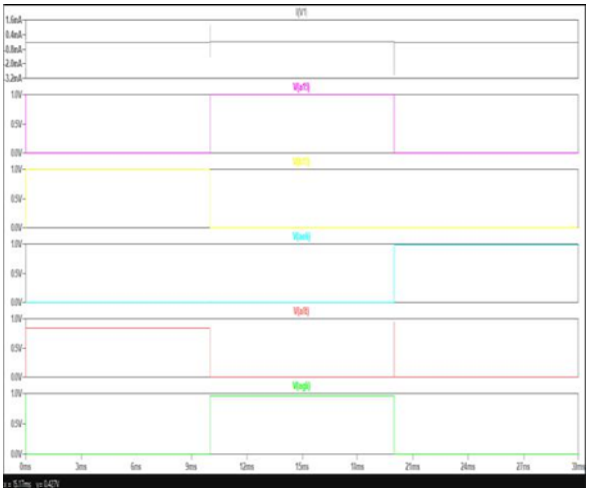

Fig. 17 waveform of 16-bit comparator using EXOR/EXNOR gate

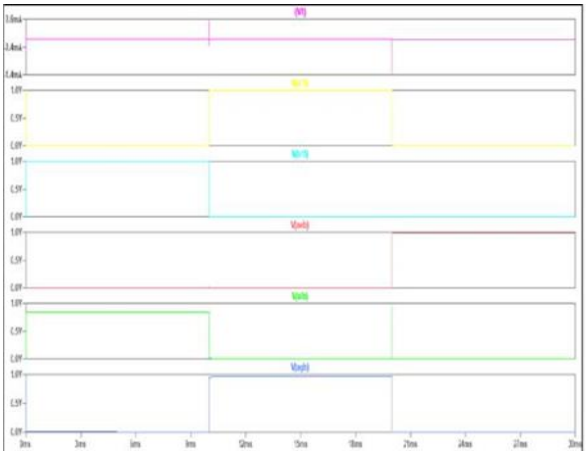

Fig. 18 waveform of 16-bit comparator using EXOR/EXNOR [1] gate

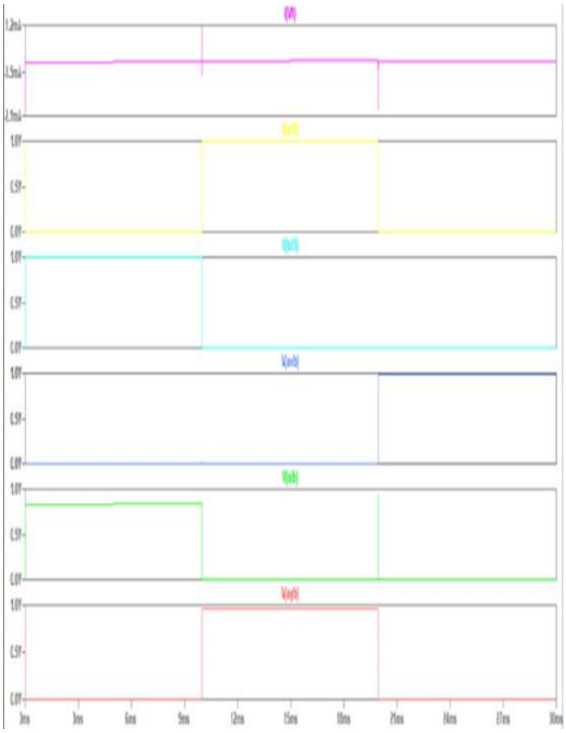

Fig. 19 waveform of 16-bit comparator using EXOR/EXNOR [3] gate

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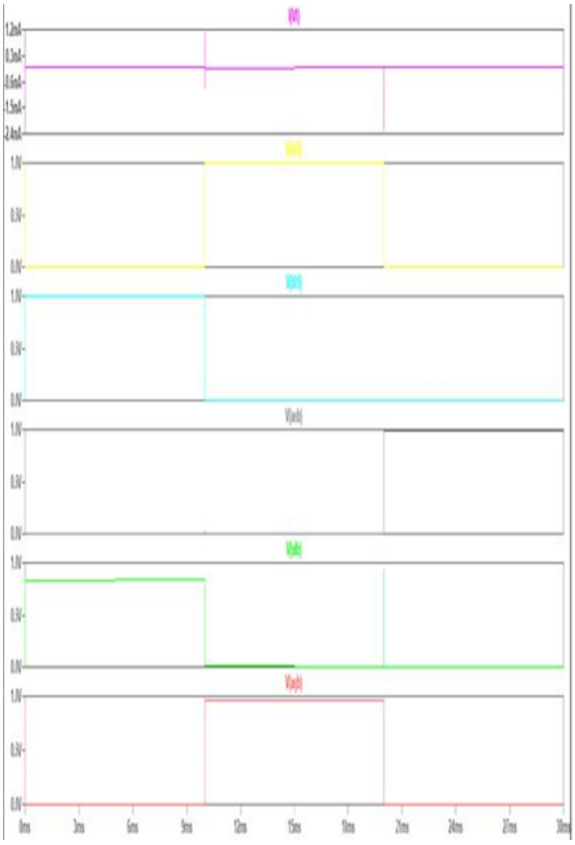

Fig. 20 waveform of 16-bit comparator using EXOR/EXNOR [4] gate

4.1 Propagation delay, power dissipation and current

Waveforms of the digital comparator:

EXOR/EXNOR gate using 24 transistors

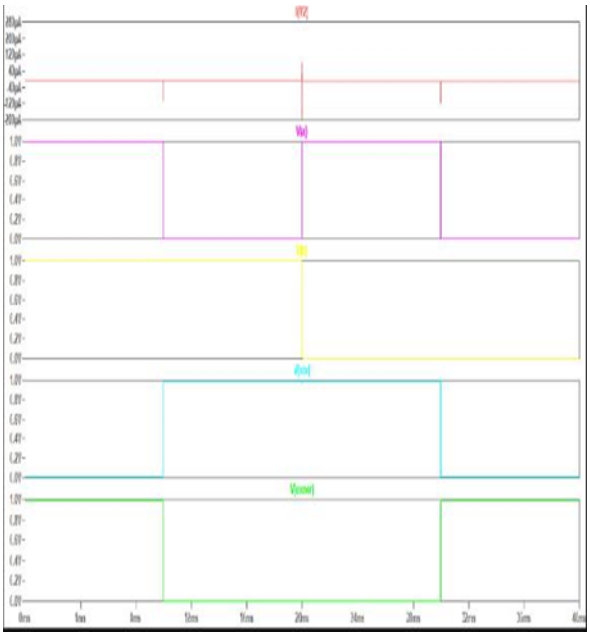

Fig. 21 waveform of EXOR/NOR gate

EXOR/NOR [1] gate

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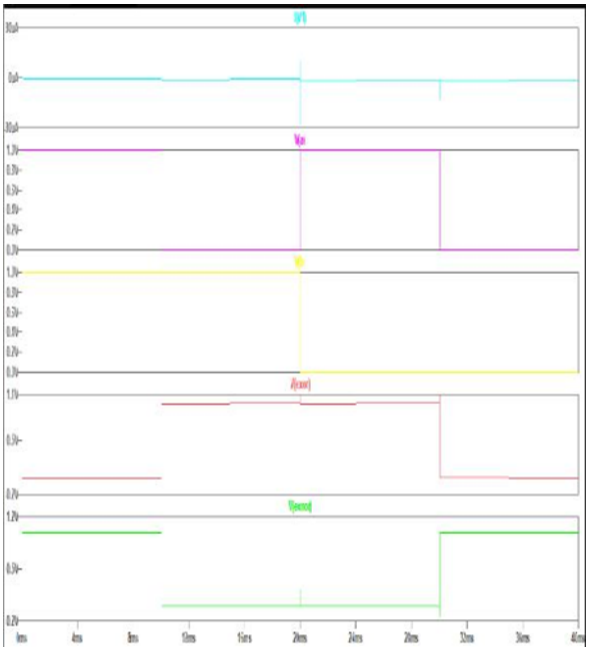

Fig. 22 waveform of EXOR/EXNOR [1] gate

EXOR/NOR [3] gate

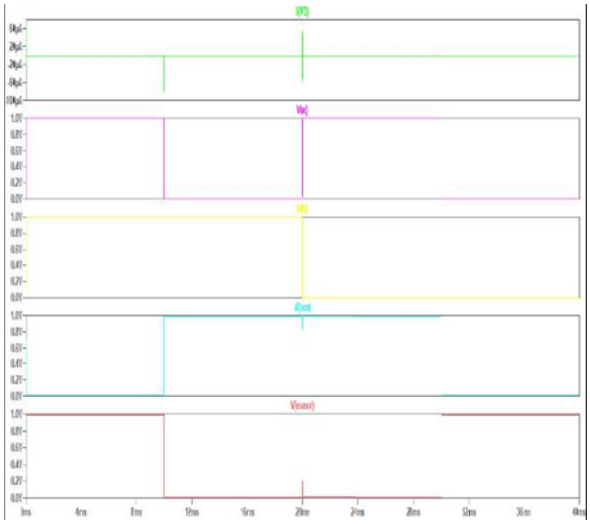

Fig. 23 waveform of EXOR/EXNOR [3] gate

EXOR/EXNOR [4] gate

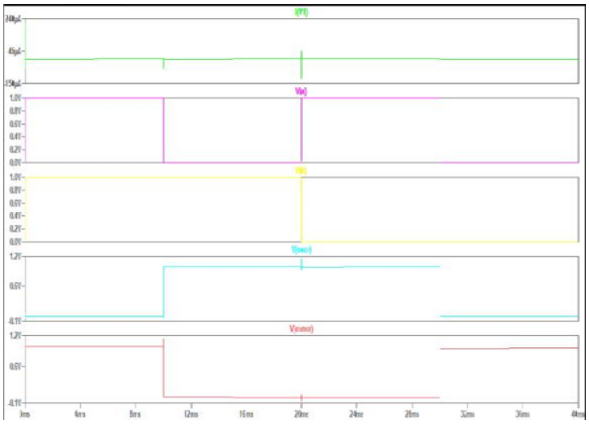

Fig. 24 waveform of EXOR/EXNOR [4] gate

Table. 1: Comparison table of EXOR/EXNOR gates

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Type of EX-OR-NOR gates	Number of Transistors	Technology used	Supply Voltage	Delay	Current	Power Dissipated
EX-OR	24	45nm	1v	61.680µs	8.5822µA	8.5822µw
EX-OR[1]	**7**	45nm	1v	92.521µs	2.619µA	2.619µw
EX-OR[3]	8	45nm	1v	**30.769µs**	2.2167µA	2.2167µw
EX-OR[4]	8	45nm	1v	61.680µs	**2.139µA**	**2.139µw**

From the above comparison table the calculated terms various EXOR/EXNOR gates is as like number of transistors and delay, current and power dissipation values. In the above comparison we are using different logic gates such as EXOR/EXNOR gate, EXOR/EXNOR [1], EXOR/EXNOR[3], EXOR/EXNOR[4]. If the number of transistors are increased then the design of the circuit will become complex. The value of the Delay becoming more when the number of transistors are increased, for the propagation delay term the operation is based on the number of the transistors. Then the next term we calculated is the value of the current, as the number of transistors are increased then the current will decrease. The power dissipation value as compared with the number of transistors are increased then the value of the power dissipation will be decreased. The above comparison is for the EXOR/EXNOR circuits which are placed in the place of the Novel EXOR gate in the 4-bit digital comparator and it also implemented in the 8-bit and the 16-bit digital comparators.

The propagation delay is calculated by using the cursors in the waveforms, this values are calculated at the position of the two inputs of the voltages applied and that values are subtracted and gives the value of the propagation delay. And now the value of the power dissipation is calculated by using the current value of the different gates and the value of power is calculated by using the current and the power supply voltage.

5. Results

Number of bits	**Typesof EX-OR Gates**	**Technology**	**Number of Transistors**	**Supply Voltage**	**Delay**	**Current**	**Power**
4-bit	Conventional EXOR	45nm	160	1v	66.152µs	51.441µA	51.441µw
	EXOR[1]	45nm	**92**	1v	44.102µs	26.751µA	26.751µw
	EXOR[3]	45nm	96	1v	**22.051µs**	25.36µA	25.36µw
	EXOR[4]	45nm	96	1v	30.841µs	22.046µA	**22.046µw**

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8-bit	Conventional EXOR	45nm	314	1v	32.397µs	111.92µA	111.92µw
	EXOR[1]	45nm	**178**	1v	21.699µs	55.291µA	55.291µw
	EXOR[3]	45nm	186	1v	**21.500µs**	52.689µA	52.689µw
	EXOR[4]	45nm	186	1v	38.61µs	44.937µA	**44.937µw**
	Conventional EXOR	45nm	622	1v	69.480µs	225.41µA	225.41µw
16-bit	EXOR[1]	45nm	**350**	1v	46.332µs	122.23µA	122.23µw
	EXOR[3]	45nm	366	1v	**44.498µs**	117.41µA	117.41µw
	EXOR[4]	45nm	366	1v	69.498µs	103.67µA	**103.67µw**

Table. 2 Comparison Table for 4-bit, 8-bit, 16-bit digital comparators.

Conclusion

In the LTspice software, we implemented the digital comparator using four different EXOR gates: the normal EXOR gate, EXOR[1], EXOR[3], and EXOR[4]. Using four different EXOR gates in 45nm CMOS technology, we have seen the simulation results of 4-bit, 8-bit, and 16-bit digital comparator. We measured the power and delay parameters and computed the transistor count. By comparing the digital comparator's properties, we were able to determine that the EXOR[4] gate is power efficient, the EXOR[3] gate is delay efficient, and the EXOR[1] gate is area efficient.

References

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